

INFORMATION  
DISCLOSURE  
STATEMENT BY APPLICANT

Sheet 1 of 2



Application Number: 10/768,754  
Filing Date: January 26, 2004  
First Named Inventor: Adrian STOICA, et al.  
Group Art Unit: Unknown  
Examiner Name: Unknown  
Attorney Docket Number: NPO-20535-2-CU

Examiner Initials

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Examiner's Signature:

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6/5/06

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PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NPO-20535-2-CU Serial No.: To be Assigned

Applicant(s): Adrian STOICA, et al.

Filing Date: Herewith

Group: Unknown

LIST OF PRIOR ART CITED BY APPLICANT  
(Use several sheets if necessary)

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3	US-5,258,947	11-02-1993	SOURGEN	365	96	12-07-1990
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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
2	Augusto, Soares J.A., and Almeida, Beltran C.F., "Analog Fault Diagnosis in Nonlinear DC Circuits with an Evolutionary Algorithm," <i>IEEE</i> , July 2000, pp. 609-616.
3	Layzell, Paul, "A New Research Tool for Intrinsic Hardware Evolution," Second International Conference, <i>ICES98</i> , Lausanne, Switzerland, Springer, September 23-25, 1998, pp. 47-56.

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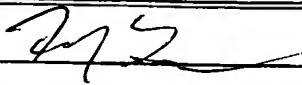
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3	Perkowski, M. Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints," <i>Proceedings of the First NASA/DoD Workshop</i> , July 19-21, 1999, pp. 129-138.
3	Stoica, Adrian, "Reconfigurable Transistor Arrays for Evolvable Hardware," <i>NASA Tech Brief</i> , Vol. 25, No. 2, Item # from JPL New Technology Report NPO-20078, July 26, 1996, pp5a.
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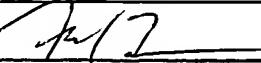
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Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
2	Stoica, A., Keymeulen, D., Zebulum, R., Thakoor, A., Daud, T., Klimeck, G., Jin, Y., Tawel, R., and Duong, V., "Evolution of analog circuits on Field Programmable Transistor Arrays," <i>IEEE</i> , July, 2000, pp. 1-10.
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